REMARKS

The applicants appreciate the Examiner's thorough examination of the application and requests reexamination and reconsideration of the application in view of the following remarks.

The Examiner indicates that claims 8-11 are allowed and that claim 6 is allowable if rewritten in independent form. Applicants would like to thank the Examiner for the indication of allowable subject material.

The subject invention results from the realization that a truly simple and effective fractional-N synthesizer with programmable output phase can be achieved by generating synchronization pulses at integer multiples of periods of the input reference signal and re-initializing the interpolator with a synchronization pulse to define the phase of the output signal or resetting the interpolator with a predetermined phase adjustment value to vary the phase of the output signal with respect to the phase of the input signal.

Claim 13 stands rejected under 35 U.S.C. 102(a) as allegedly being anticipated by prior art Fig. 1 of the subject application. Applicants herein amend claim 13 to expedite prosecution, and not for reasons related to patentability since the feature of the frequency divider was already apparent from the claim language.

In the rejection of claim 13, the Examiner alleges that the step of "scaling the accumulated fractional phase by a predetermined frequency value" is performed by summing circuit 24 and that "loading the predetermined phase value into an interpolator to define a predetermined output frequency and phase" is performed by the programmable divider 22. Although the applicants disagree with the Examiner's interpretation of Fig. 1, specifically because the Examiner's interpretation of Fig. 1 would leave the fractional-N synthesizer without a divider, applicants herein amend claim 13 to specifically recite that the interpolator provides an

output to a frequency divider. Thus, this amendment clearly traverses the Examiner's interpretation of Fig. 1 of the subject application. The applicants' respectfully request that the Examiner withdraw the rejection of claim 13 under 35 U.S.C. §102(a).

Claim 15 stands rejected under 35 U.S.C. 102(e) as allegedly being anticipated by U.S. Patent No. 6,556,086 B2 to *Keaveney et al.*

In support of the rejection of claim 15, the Examiner alleges that *Keaveney et al.* teaches that in fractional-N synthesizers, the output signal F out is only in phase with the input reference frequency every M periods of the reference signal. To support this, the Examiner cites Col. 3, lines 34-59 of *Keaveney et al.* However, this section of *Keaveney et al.* relates to fractional-N synthesizers that are prior art to the invention of *Keaveney et al.* and not descriptive of the invention of *Keaveney et al.* itself, nor is it descriptive of Fig. 1 of *Keaveney et al.* In fact, the invention of *Keaveney et al.* overcomes the problems with the prior art by generating a synchronization pulse at integer multiples of periods of the reference signal. See *Keaveney et al.* at Col. 2, lines 1-33. Thus, in the rejection of claim 15, the Examiner is combining the invention of *Keaveney et al.* with the cited prior art of *Keaveney et al.*, when *Keaveney et al.* specifically teaches away from its cited prior art.

As further evidence of this distinction, the subject patent application at page 4, lines 2-9, teaches that for fractional-N synthesizers made prior to fractional-N synthesizer of *Keaveney et al.*, a major disadvantage is that the output phase can have any one of M possible values with respect to the input reference phase, where M is the fractional modulus. Which one of the M edges of the reference this will be may be different each time the channel is synthesized depending on the particular state of the interpolator when the new N and F values, which specify the channel to be synthesized, are loaded. In some applications this doesn't matter but when it is

required that a particular output frequency signal has consistently the same phase relationship with a reference then this is a problem with a fractional-N synthesizer.

To overcome the disadvantages of the prior art, the fractional-N synthesizer of *Keaveney et al.* synchronizes the phase output signal with the input reference signal. To accomplish this, the fractional-N synthesizer of *Keaveney et al.* generates a synchronization pulse at integer multiples of periods of the input reference signal and gates one of those synchronization pulses to re-initialize the interpolator of the fractional-N synthesizer in order to synchronize the phase of the output signal with the input reference signal. The design of the *Keaveney et al.* produces an output signal with a resultant phase which is phase locked to the input reference signal for channels at the same frequency. One drawback of the design of *Keaveney et al.* is that it cannot be programmed to vary phase of the output signal with respect to the phase of the input reference signal as claimed by applicants. *See* the subject application at page 4, line 10 to page 5, line 6. *See also Keaveney et al.* at column 2, lines 1-25.

Claim 15 as recited by the applicants includes the step of "generating a synchronization pulse at integer multiples of periods of the input reference signal". The feature of generating synchronization pulses was taught by *Keaveney et al.*, but not its cited prior art. As noted above, the apparatus of *Keaveney et al.* includes the noted disadvantage that it can not be programmed to vary the phase of the output signal with respect to the phase of the input signal. As such, the subject invention of claim 15 includes the step of "generating an enable signal to reset an interpolator of said fractional-N synthesizer with said predetermined phase to vary the phase of said output signal with respect to the phase of said input reference signal". As such, claim 15 clearly distinguishes over *Keaveney et al.* and also over the prior art cited in *Keaveney et al.*

Accordingly, claim 15 is patentable over *Keaveney et al.* Applicants respectfully request

that the Examiner withdraw the rejection of claim 15 under 35 U.S.C. 102(e).

Claims 1-5, 7, 12 and 14 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable by by prior art Fig. 1 of the subject application in view of U.S. Patent Application No. 2002/1091727 to *Staszewski et al.*

As the Examiner correctly notes in paragraph 5 on page 6 of the Office Action, Fig. 1 of the subject application does not disclose the feature of a phase adjustment circuit responsive to a synchronization circuit for varying the phase of the output signal with respect to the input reference signal. Fig. 1 of the subject application also does not disclose the feature of claim 14 that recites "applying a fractional value and a modified fractional value selectively applying a fractional value and a modified fractional value to an interpolator of said fractional-N synthesizer to define a predetermined phase relationship between said output signal and said input reference signal".

To overcome the deficiencies of Fig. 1 of the subject application, the Examiner combines it with *Staszewski et al. Staszewski et al.,* however, also fails to teach these features of the applicants' claimed invention and therefore the combination of Fig. 1 with *Staszewski et al.* does not disclose the subject invention as claimed by the applicants. *Staszewski et al.* fails to disclose the applicants' claimed synchronization circuit that is responsive to the input reference signal for generating synchronization pulses at integer multiples of M periods of the input reference signal. *Staszewski et al.* also fails to disclose a phase adjustment circuit responsive to the applicants' claimed synchronization circuit for varying the phase of the output signal with respect to the input reference signal.

In fact, not only does *Staszewski et al.* not disclose the applicants' claimed phase adjustment circuit, *Staszewski et al.* clearly teaches away from the invention as claimed by the

applicants. Referring to Fig. 5 of *Staszewski et al.*, its synthesizer 80 includes a rising fractional phase error circuit 64a and a falling fractional phase error circuit 64b. Error circuits 64a and 64b are for better locking the input signal to the output signal by not only determining the error on the rising edge of the reference frequency, but also on the falling edge of the reference frequency by using error circuit 64b. Thus, rather than varying the phase of the output signal with respect to the input reference signal, the disclosure of *Staszewski et al.* teaches that it is not just desirable to lock the phase between the input and output signals, that two error circuits 64a and 64b should be used to determine the error to thereby better lock the phase of the input and output signals.

Moreover, one skilled in the art would not even look to combine Fig. 1 with *Staszewski et al.* because they relate to significantly different circuits. In contrast to Fig. 1 of the subject invention, *Staszewski et al.* relates only to a direct digital synthesizer but not a fractional-N synthesizer.

In a typical fractional-N synthesizer, the divider in the feedback path has an integer and fractional part and the output frequency step resolution is a fraction of the reference frequency, as shown in equation 1:

$$f_{OUT} = \left(N + \frac{F}{M}\right) \times f_{REF} \qquad (1)$$

The fractional part is generated using a digital interpolator. This outputs a sequence of integer values with an average value given by F/M where F is the input fraction and M is the modulus. *See* the subject application at page 2, line 25 to page 3, line 7.

Staszewski et al. does not disclose such a fractional-N synthesizer in which the divider in the feedback path includes an integer and a fractional part. Rather, *Staszewski et al.* discloses a synthesizer in which the output frequency of the synthesizer is $f_{OUT} = f_{REF} \times N$. See Figs. 1, 3a, 8

of *Staszewski et al.* Since *Staszewski et al.* does not disclose or relate to a fractional-N synthesizer, it also does not suffer from the same disadvantages of prior fractional-N synthesizers as described above. Thus, one skilled in the art would not even look to combine *Staszewski et al.* with Fig. 1 of the subject application in the first place.

In summary, not only does the combination of Fig. 1 and *Staszewski et al.* fail to disclose the subject invention, *Staszewski et al.* teaches away from the subject invention, and one skilled in the art would not even look to combine these two references in the first place.

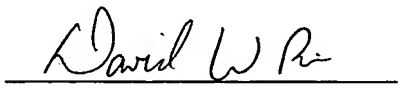
Accordingly, applicants respectfully request that the Examiner withdraw the rejection of claims 1-5, 7, 12 and 14 under 35 U.S.C. 103(a)

CONCLUSION

Each of the Examiner's rejections has been addressed or traversed. It is respectfully submitted that the application is in condition for allowance. Early and favorable action is respectfully requested.

If for any reason this Response is found to be incomplete, or if at any time it appears that a telephone conference with counsel would help advance prosecution, please telephone the undersigned or his associates, collect in Waltham, Massachusetts at (781) 890-5678.

Respectfully submitted,



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